

**7A, 300V N-CHANNEL POWER MOSFET**

**GENERAL DESCRIPTION**

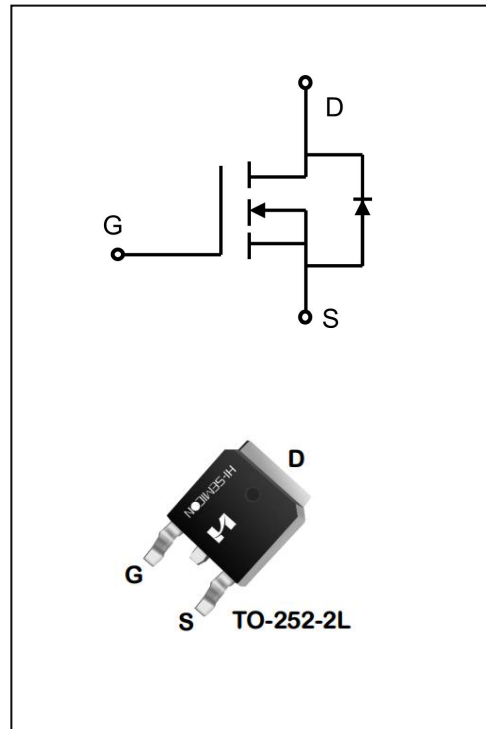
These N-Channel enhancement mode power field effect transistors are produced using Hi-semicon's proprietary, planar stripe, VDMOS technology.

**Features**

- ◆  $V_{DS}(V)=300V, I_D=7A$
- ◆  $R_{DS(on)}$   
 TYP:  $520m\Omega @ V_{GS}=10V, I_D=3.5A$   
 MAX:  $600m\Omega$

**Applications**

- ◆ Power faction correction (PFC)
- ◆ Switched mode power supplies (SMPS)
- ◆ Uninterruptible power supply (UPS)
- ◆ LED lighting power



**ORDERING INFORMATION**

Part No.	Package	Marking	Material	Packing
SFD7N30TS	TO-252-2L	SFD7N30TS	Pb free	Reel

## ABSOLUTE MAXIMUM RATINGS (T<sub>J</sub>=25°C unless otherwise noted)

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	300	V
Gate-Source Voltage	V <sub>GS</sub>	±30	V
Drain Current	I <sub>D</sub>	T <sub>C</sub> = 25°C	7.0
		T <sub>C</sub> = 100°C	4.8
Drain Current Pulsed (Note 1)	I <sub>DM</sub>	28	A
Power Dissipation(T <sub>C</sub> =25°C) -Derate above 25°C	P <sub>D</sub>	76	W
		0.61	W/°C
Single Pulsed Avalanche Energy (Note 2)	E <sub>AS</sub>	320	mJ
Operation Junction Temperature Range	T <sub>J</sub>	-55~+150	°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	TL	300	°C

## THERMAL CHARACTERISTICS

Characteristics	Symbol	MAX	Unit
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.6	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W

## ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain -Source Breakdown Voltage	B <sub>VDS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	300	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =300V, V <sub>GS</sub> =0V	--	--	100	nA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =30V, V <sub>DS</sub> =0V	--	--	100	nA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V	--	--	-100	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0	3.0	4.0	V
Static Drain- Source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A	--	520	600	mΩ
<b>Dynamic Characteristics</b>						
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> =0V; f=1.0MHZ	--	4.0	--	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V V <sub>GS</sub> =0V f=1.0MHZ	--	455	--	pF
Output Capacitance	C <sub>oss</sub>		--	70	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	10.6	--	
<b>Switching Characteristics</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =180V R <sub>G</sub> =25Ω I <sub>D</sub> =7A (Note 3.4)	--	13.1	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	26.4	--	

Turn-off Delay Time	$t_{d(off)}$	$V_{DD}=180V$ $R_G=25\Omega$	--	20.6	--	ns
Turn-off Fall Time	$t_f$	$I_D=7A$ (Note 3.4)	--	24.1	--	
Total Gate Charge	$Q_g$	$V_{DS}=240V, I_D=7A$ $V_{GS}=10V$ (Note 3.4)	--	11.7	--	nC
Gate-Source Charge	$Q_{gs}$		--	4.04	--	
Gate-Drain Charge	$Q_{gd}$		--	5.37	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7	A
Pulsed Source Current	$I_{SM}$		--	--	28	
Diode Forward Voltage	$V_{SD}$	$I_S=7A, V_{GS}=0V$	--	1.0	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_F=7A, V_R=300V,$ $dI_F/dt=100A/\mu S$	--	44.6	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	59.6	--	nC

1. Pulse width limited by maximum junction temperature
2.  $L=10mH, I_{AS}=8.0A, V_{DD}=100V, V_G=10V, R_G=25\Omega,$  starting  $T_J=25^\circ C$
3. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

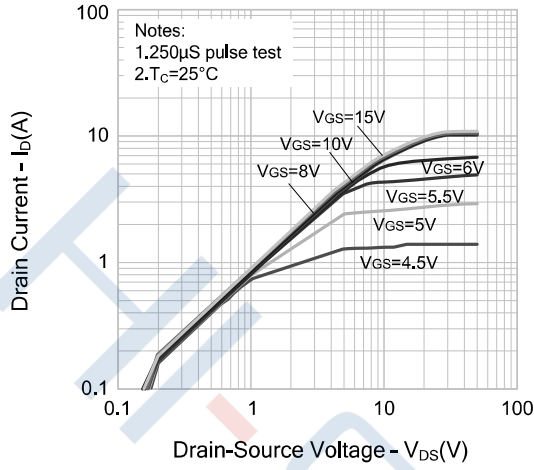


Figure 2. Transfer Characteristics

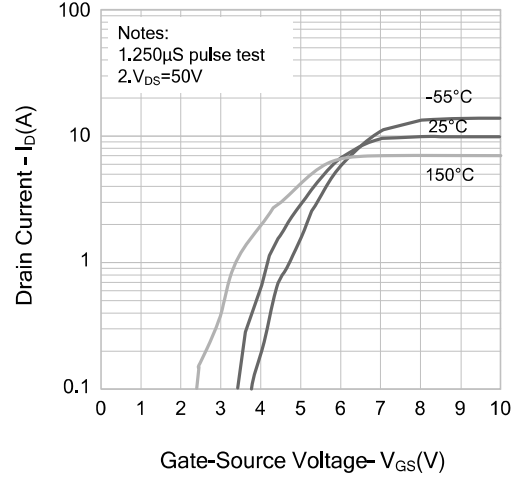


Figure 3. On-Resistance Variation vs. Drain Current

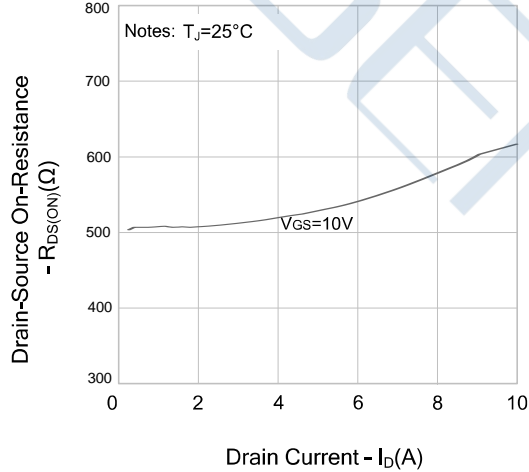


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

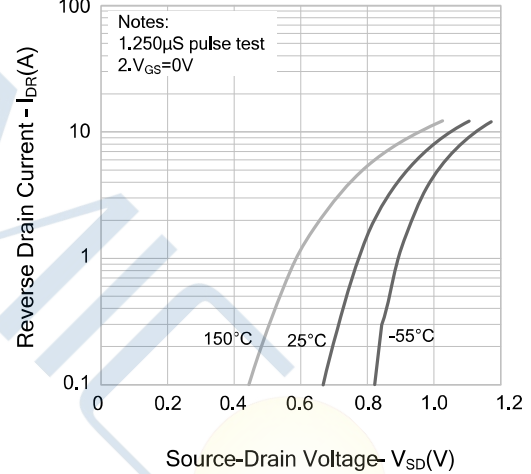


Figure 5. Capacitance Characteristics

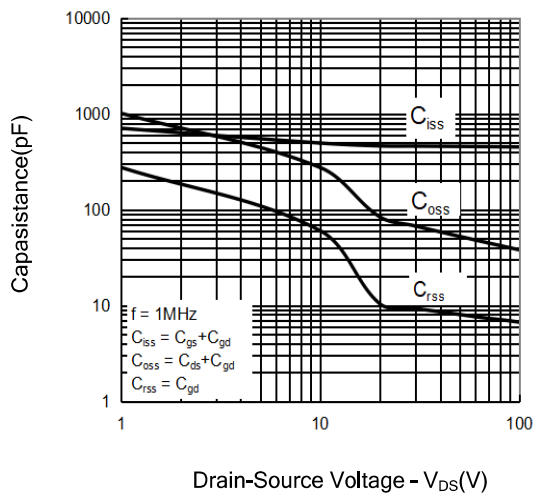
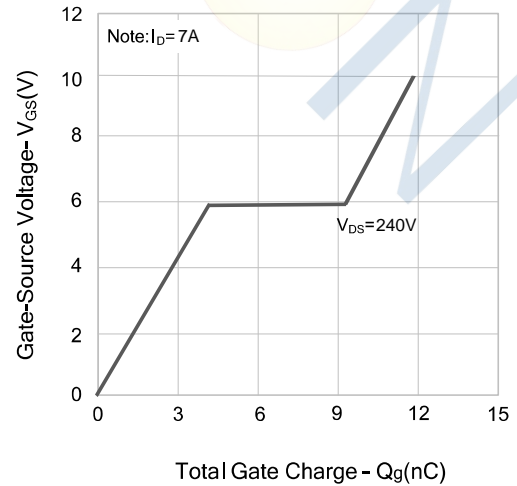


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Variation vs. Temperature

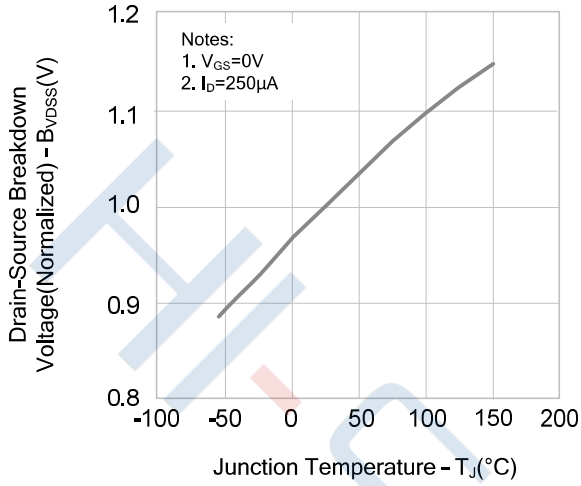


Figure 8. On-resistance Variation vs. Temperature

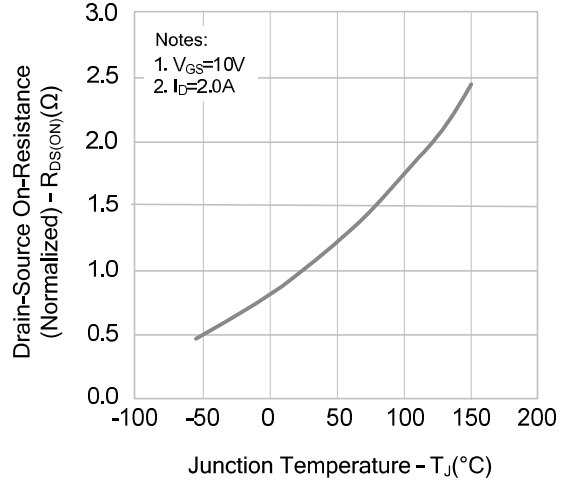


Figure 9 . Max. Safe Operating Area

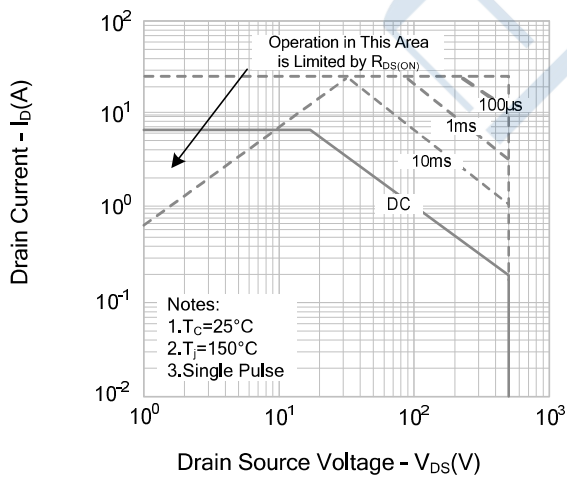
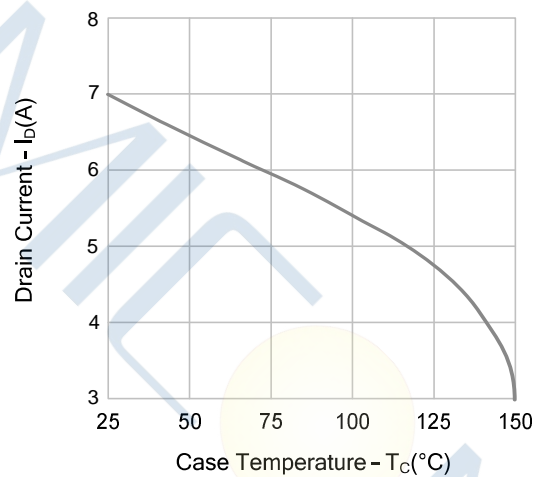
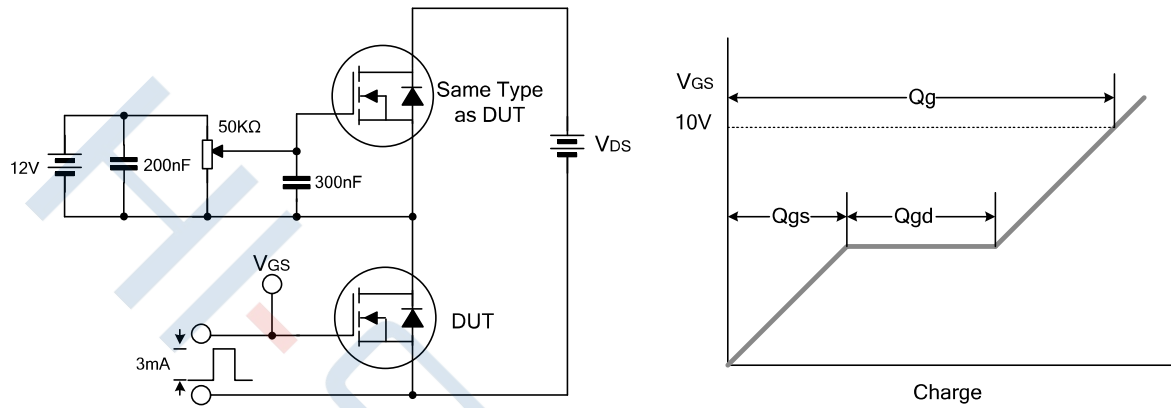


Figure 10. Maximum Drain Current vs. Case Temperature

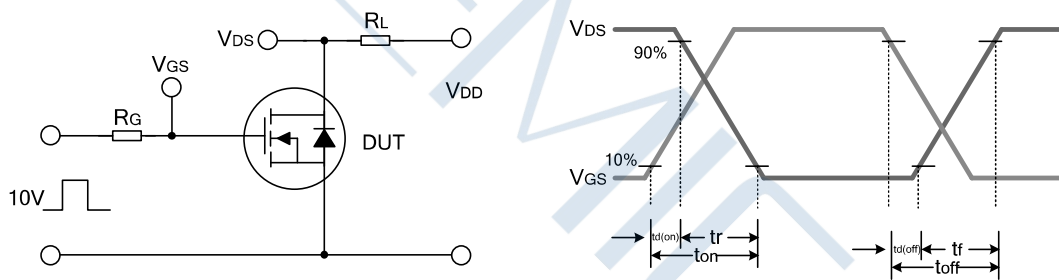


Test Circuit

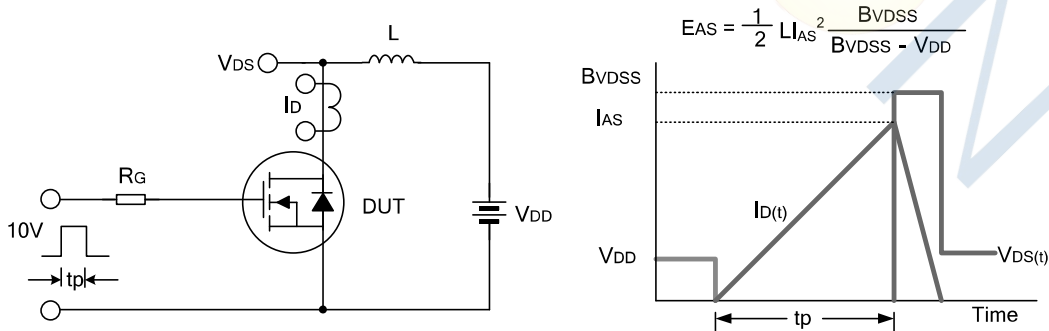
Gate Charge Test Circuit & Waveform



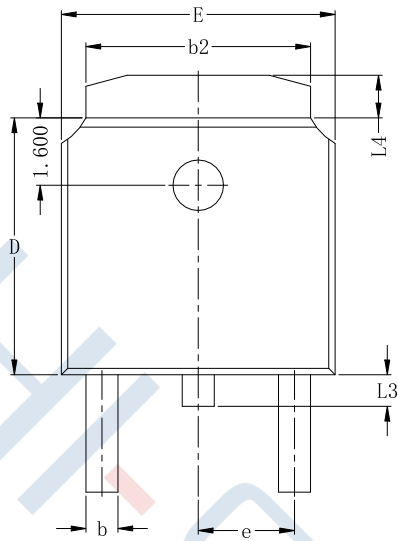
Resistive Switching Test Circuit & Waveform



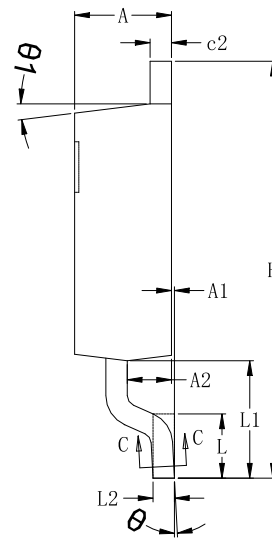
Undamped Inductive Switching Test Circuit & Waveform



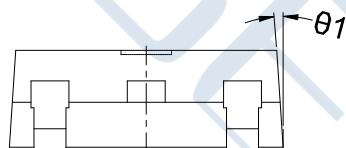
Package Dimensions of TO-252-2L



TOP VIEW



SIDE VIEW (Right)



SIDE VIEW (Front)

DIM SYMBOL	MIN.	NOM.	MAX.
A	2.200	2.300	2.400
A1	0.000	0.070	0.130
A2	0.950	1.050	1.150
b	0.700	0.800	0.900
b1	0.660	0.760	0.860
b2	5.134	5.334	5.534
c	0.448	0.548	0.648
c1	0.458	0.508	0.558
c2	0.448	0.548	0.648
D	6.000	6.100	6.200
D2	5.372	5.572	5.772
E	6.400	6.500	6.600
E2	4.900	5.100	5.300
e	2.286 BSC.		
H	9.700	9.900	10.100
L	1.380	1.525	1.725
L1	2.588	2.788	2.988
L2	0.508 BSC.		
L3	0.600	0.750	0.950
L4	0.812	1.012	1.212
theta	1°	3°	5°
theta1	6°	7°	8°

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