

N-Ch and P-Ch Power MOSFET

GENERAL DESCRIPTION

Complementary Enhancement MOSFET in a PDFN5*6 Package. The SFM0318T4 uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge can be used in a wide variety of applications.

Features

- ◆ N-CHANNEL

$V_{DS}=30V, I_D=23A$

$R_{DS(on)(TYP)}=15m\Omega ; (VGS=10V)$

$R_{DS(on)(TYP)}=20m\Omega ; (VGS=4.5V)$

- ◆ P-CHANNEL

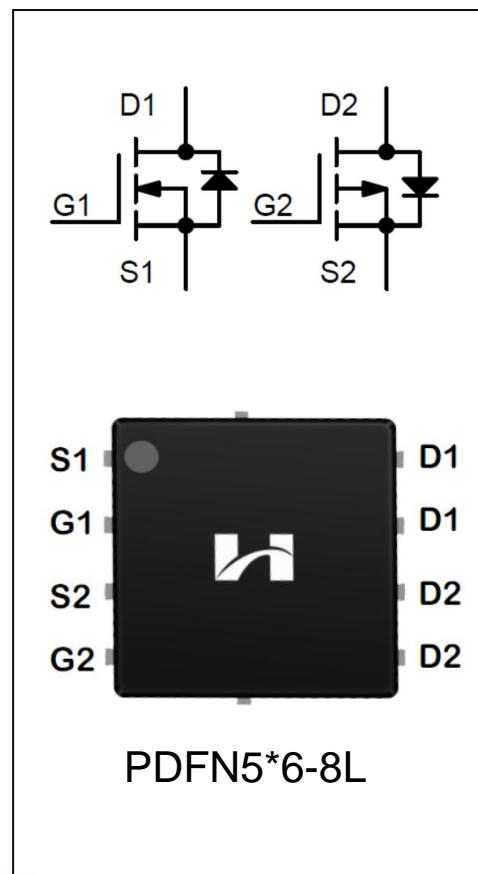
$V_{DS}=-30V, I_D=-18A$

$R_{DS(on)(TYP)}=24m\Omega ; (VGS=-10V)$

$R_{DS(on)(TYP)}=35m\Omega ; (VGS=-4.5V)$

Applications

- ◆ Power factor correction (PFC)
- ◆ Switched mode power supplies (SMPS)
- ◆ Uninterruptible power supply (UPS)
- ◆ LED lighting power



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFM0318T4	PDFN 5*6-8L	SFM0318T4	Pb Free	Reel

ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	N-CHANNEL	P-CHANNEL	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Drain Current	I_D	23	-18	A
		14	-12	
Drain Current Pulsed(Note 1)	I_{DM}	40	-36	A
Power Dissipation($T_C=25^\circ\text{C}$)	P_D	3.6		W
Operation Junction Temperature Range	T_J	-55 to +150		$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150		$^\circ\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	TL	300		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	MAX	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	34	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	180	$^\circ\text{C/W}$

N-Ch ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain -Source Breakdown Voltage	B_{VDSS}	$V_{GS}=0V, I_D=250\mu A$	30	33	--	V
Drain-Source Leakage Current	I_{DS}	$V_{DS}=30V, V_{GS}=0V$	--	--	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	--	--	100	nA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	--	--	-100	
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1	1.5	2.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8A$	--	15	20	$m\Omega$
		$V_{GS}=4.5V, I_D=5A$	--	20	27	$m\Omega$
Forward Transconductance	g_F	$V_{DS}=10V, I_D=5A$		6.5		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=15V$ $V_{GS}=0V$ $f=1.0MHz$	--	850	--	pF
Output Capacitance	C_{oss}		--	65	--	
Reverse Transfer Capacitance	C_{rss}		--	58	--	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V; V_{GS}=10V$ $R_G=3.3\Omega I_D=3A$ (Note 2.3)	--	5.1	--	nS
Turn-on Rise Time	t_r		--	3.2	--	
Turn-off Delay Time	$t_{d(off)}$		--	13.5	--	
Turn-off Fall Time	t_f		--	3.7	--	
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=3A$ $V_{GS}=10V$ (Note 2.3)	--	15.5	--	nC
Gate-Source Charge	Q_{gs}		--	2.3	--	
Gate-Drain Charge	Q_{gd}		--	3.5	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_s	Integral Reverse P-N Junction Diode in the MOSFET	--	--	20	A
Pulsed Source Current	I_{SM}		--	--	40	
Diode Forward Voltage	V_{SD}	$I_s=20A, V_{GS}=0V$	--	0.81	1.2	V

NOTE:

1. Pulse width limited by maximum junction temperature
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
3. Essentially independent of operating temperature

P-Ch ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain -Source Breakdown Voltage	V_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	--	--	V
Drain-Source Leakage Current	I_{DS}	$V_{DS}=-30V, V_{GS}=0V$	--	--	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	--	--	100	nA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	--	--	-100	
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1	-1.5	-2.5	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-8A$	--	24	30	$m\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	--	35	43	$m\Omega$
Forward Transconductance	g_F	$V_{DS}=-5V, I_D=10A$		11		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=-15V$ $V_{GS}=0V$ $f=1.0MHz$	--	860	--	pF
Output Capacitance	C_{oss}		--	390	--	
Reverse Transfer Capacitance	C_{rss}		--	180	--	
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V; V_{GS}=-10V$ $R_G=3.0\Omega I_D=-15A$ (Note 2.3)	--	6.9	--	nS
Turn-on Rise Time	t_r		--	18	--	
Turn-off Delay Time	$t_{d(off)}$		--	21	--	
Turn-off Fall Time	t_f		--	8.5	--	
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-15A$ $V_{GS}=-10V$ (Note 2.3)	--	16.6	--	nC
Gate-Source Charge	Q_{gs}		--	3.8	--	
Gate-Drain Charge	Q_{gd}		--	6.6	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_s	Integral Reverse P-N Junction Diode in the MOSFET	--	--	-18	A
Pulsed Source Current	I_{SM}		--	--	-36	
Diode Forward Voltage	V_{SD}		--	-0.85	-1.4	V

NOTE:

1. Pulse width limited by maximum junction temperature
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
3. Essentially independent of operating temperature

N-Channel Typical Performance Characteristics

Figure 1. Output Characteristics

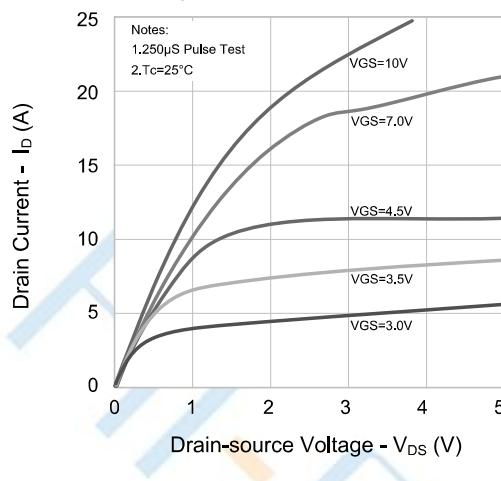


Figure 2. Transfer Characteristics

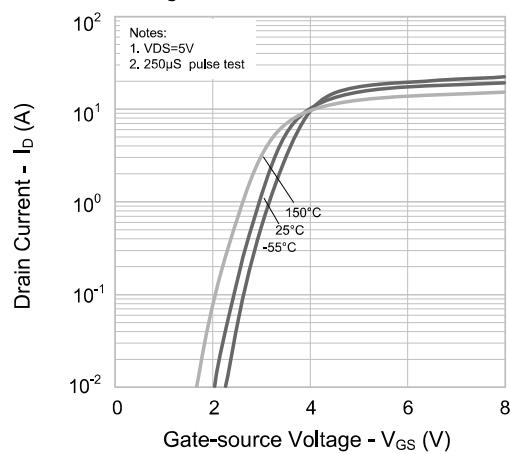


Figure 3. On-resistance vs. Drain Current

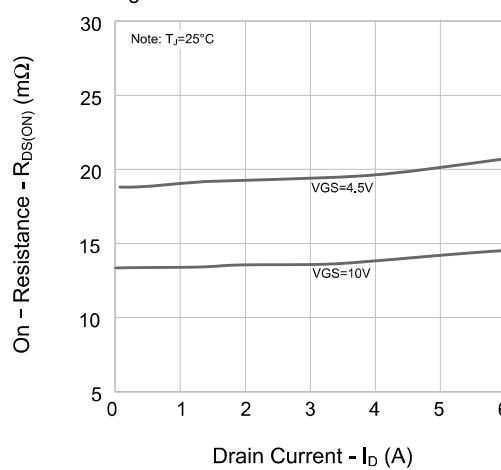


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

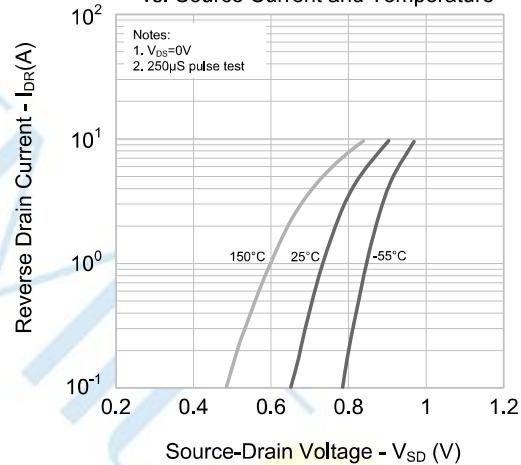


Figure 5. Capacitance Characteristics

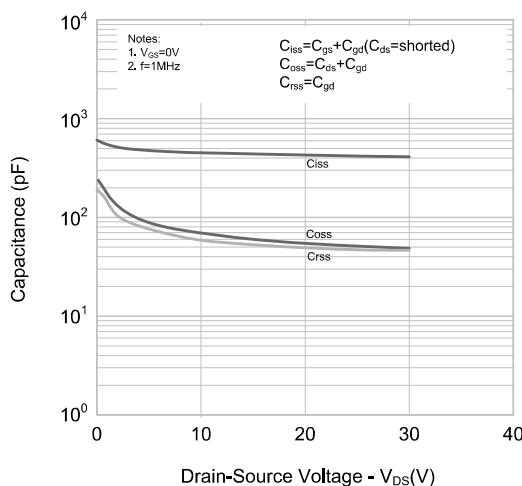
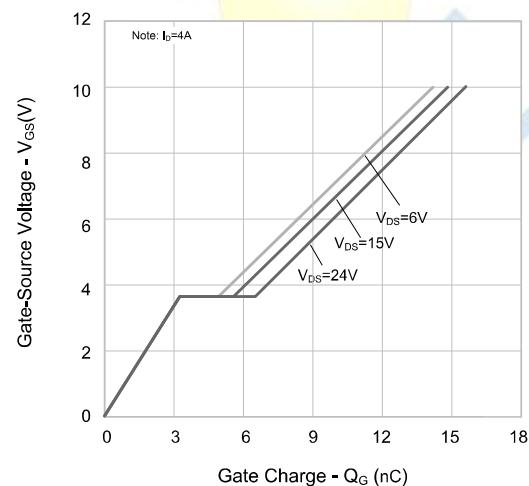


Figure 6. Gate Charge



P-Channel Typical Performance Characteristics

Figure 1.On-Region Characteristics

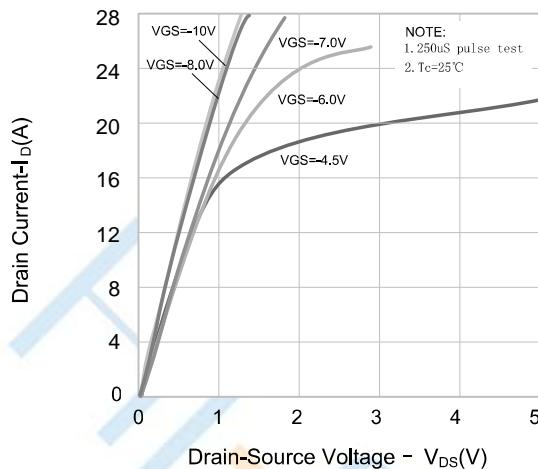


Figure 2.Transfer Characteristics

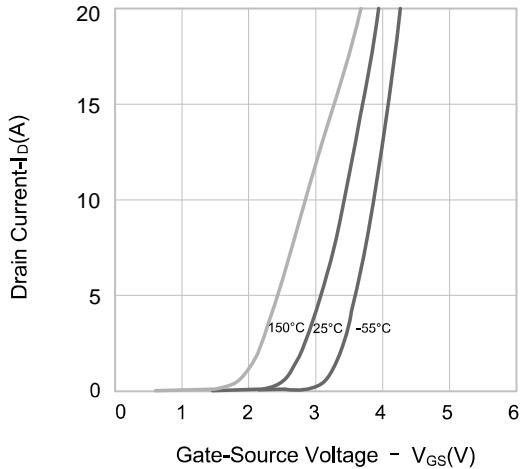


Figure 3.On-Resistance Variation vs. Drain-Current, Gate Voltage

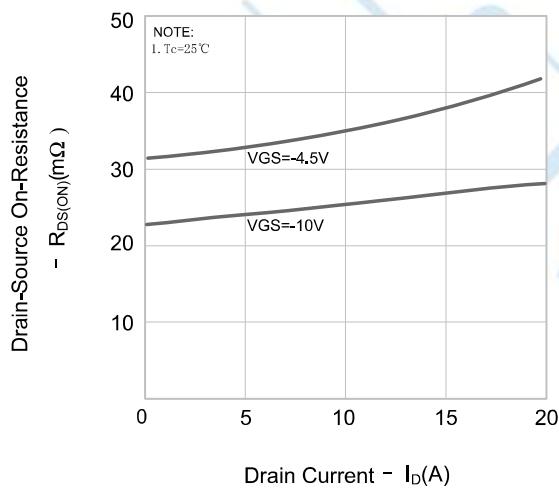


Figure 4.Body Diode Forward Voltage Variation vs. Source Current and Temperature

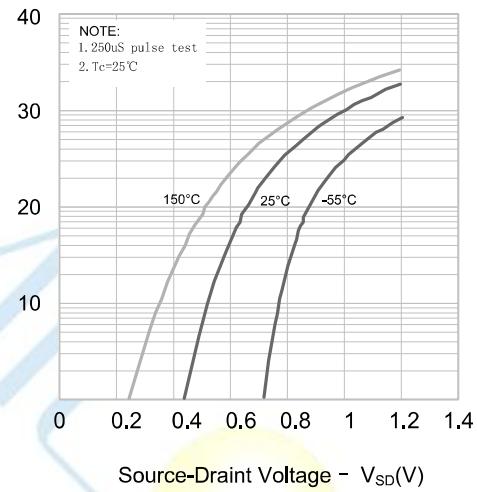


Figure 5.Capacitance Characteristics

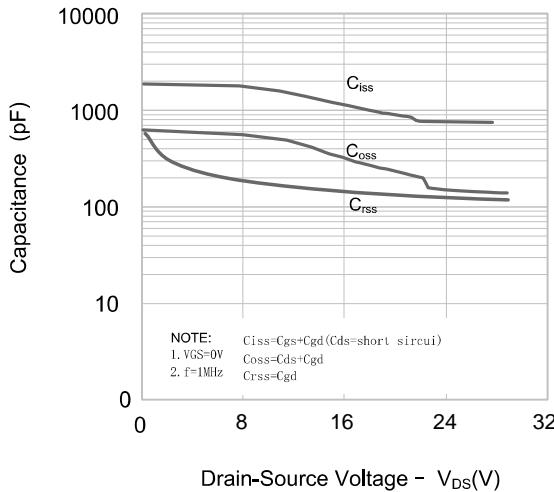
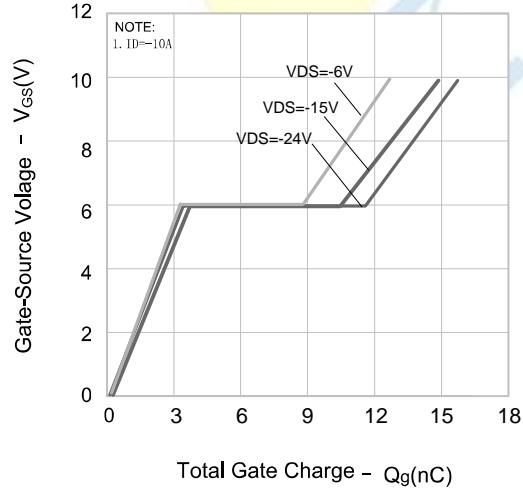


Figure 6.Gate Charge Characteristics



P-Channel Typical Performance Characteristics

Figure 7. Breakdown Voltage Variation vs.Temperature

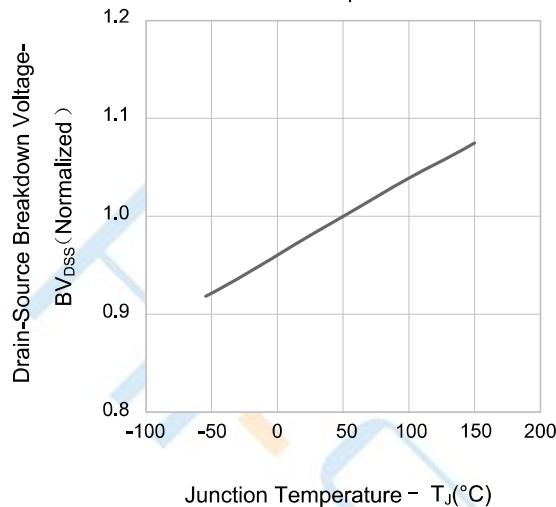


Figure 8.On-resistance Variation vs.Temperature

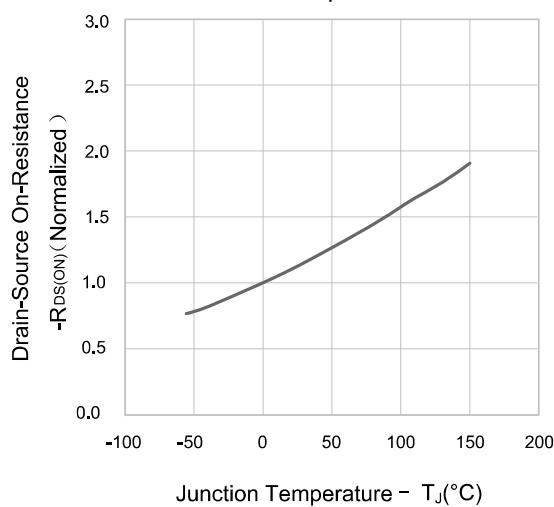
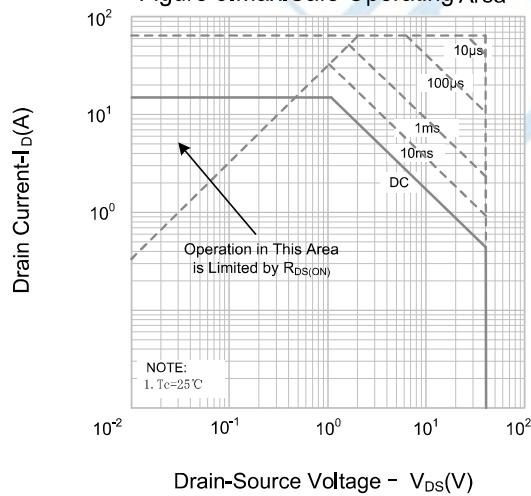
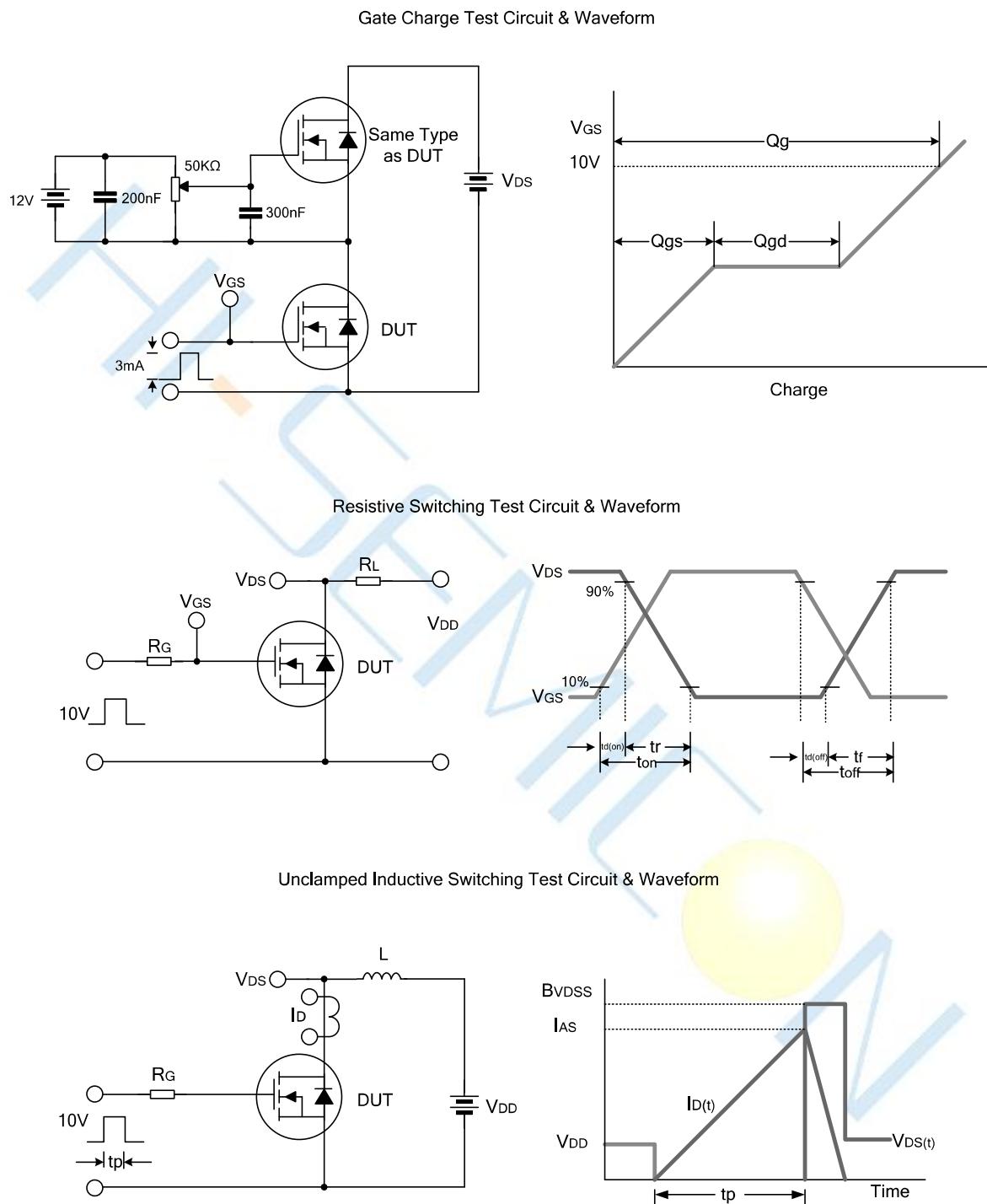


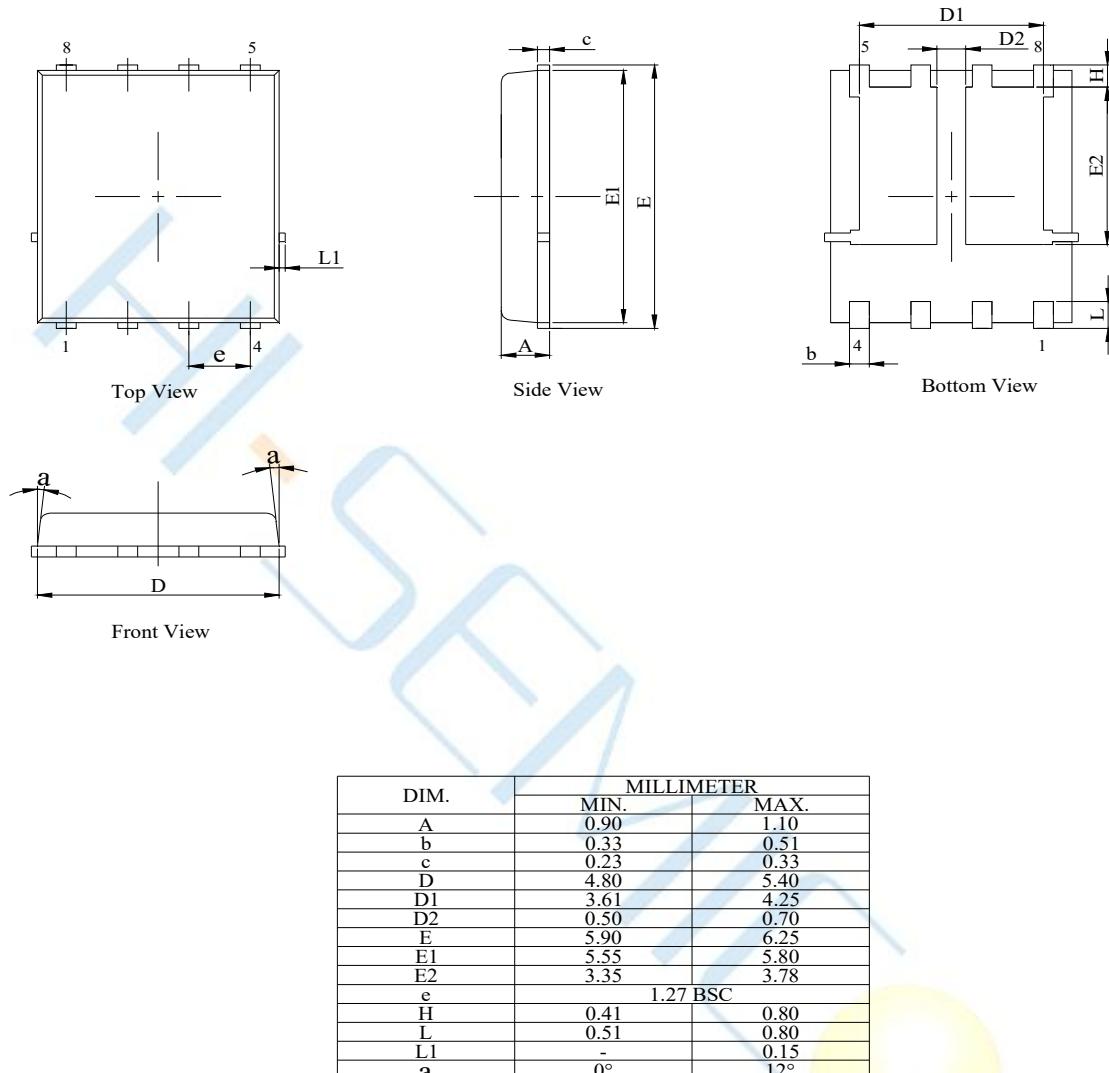
Figure 9.Max.Safe Operating Area



Test Circuit



Package Dimensions of PDFN5*6-8L



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